Memory System Organization & Architecture

Module 4

Outline

- Internal Organization of Memory Chip
- Organization of a SRAM memory unit
- Design of memory modules

Memory

- It's all about storing bits – binary digits
- Vacuum tubes, CRT, Drums, Disks and ICs
- Issues – size, cost and speed
- Semiconductor memories (Chips)

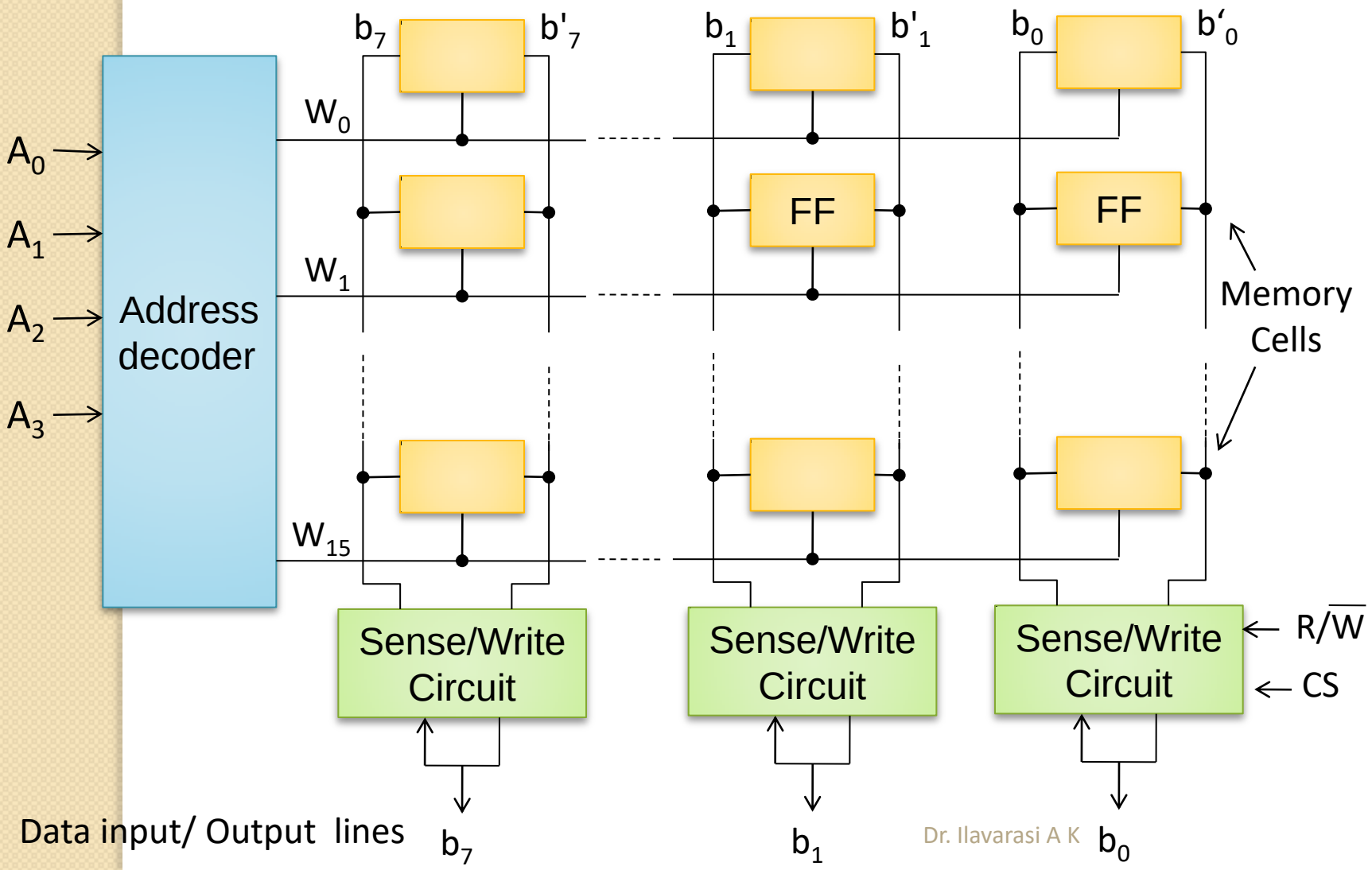
Terminology

- *Memory Access Time*: Time between read and the MFC (Memory Function Complete) signal.
- *Memory Cycle Time*: The minimum time delay required between the initiation of two successive memory operations.
- *Random Access Memory (RAM)*: Any location can be accessed for a read or write operation in some fixed amount of time that is independent of the location's address.

Semiconductor RAM Memories

- Semiconductor memories are available in a wide range of speeds.
- Their cycle time range from 100ns to less than 10ns.
- Obviously the speed of the processor depends on the speed of the memory

Internal Organization of Memory Cells

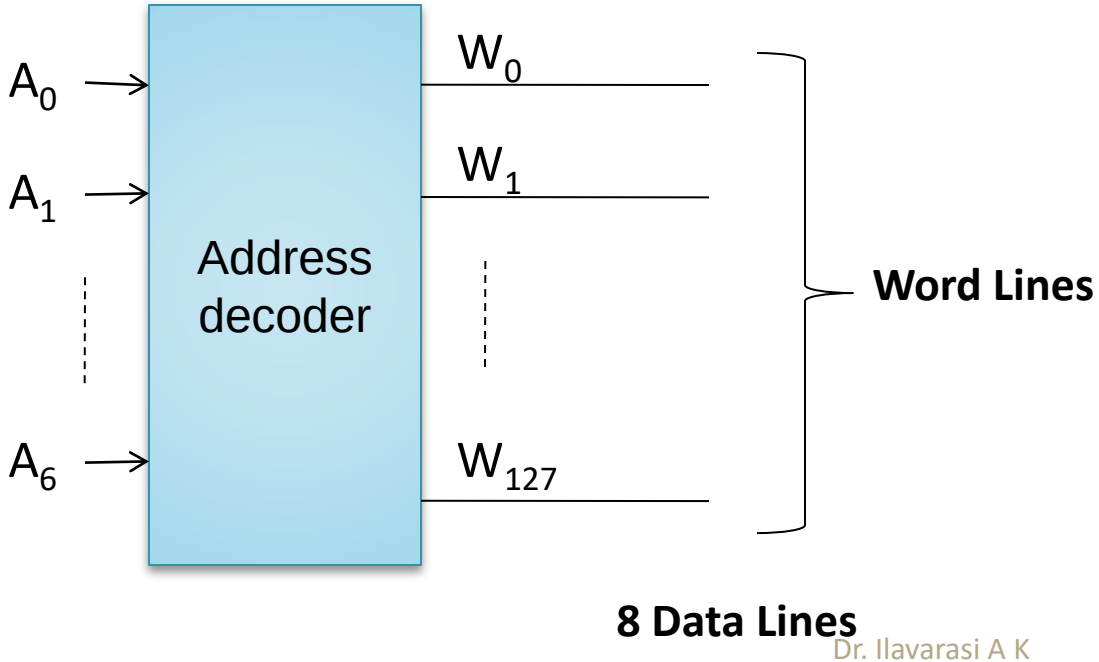


Internal Organization of Memory Cells

- Above Example: 128 bit chip
  - It has 4 address lines and 8 data lines
  - Using 4 address lines ($A_3A_2A_1A_0$) 16 word signals ($W_{15}\ldots W_1W_0$) are generated with help of decoder 4:16 decoder
  - 16 words of each 8 bits (= 16 x 8 bits = 16 bytes)
  - For any given input address lines ($A_3A_2A_1A_0$) only one of the word lines from W_{15} … W_0 will be active at a time.
  - Which in turn enable the complete row of the memory cells connected to W_i bit
  - Using R/W and CS signal one can enable the Sense/Write Circuits of the all bits ranging from b_7 to b_0

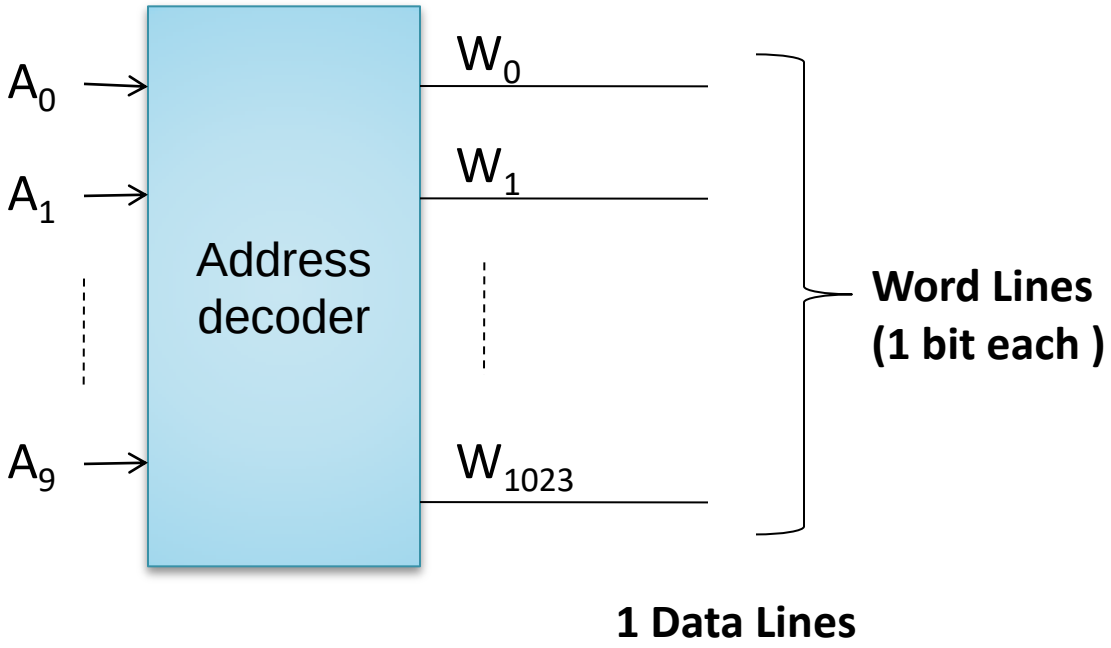
Chip with 1024 Memory Cells

- 1024 bits can be planned as 128 x 8 memory
- Total address lines required 128 = 2^N → N = $\log_2 128$ =7, it means it should have A6 .. $A_1 A_0$
- It means 128 x 8 bits (Similar to 16 x 8 bits)

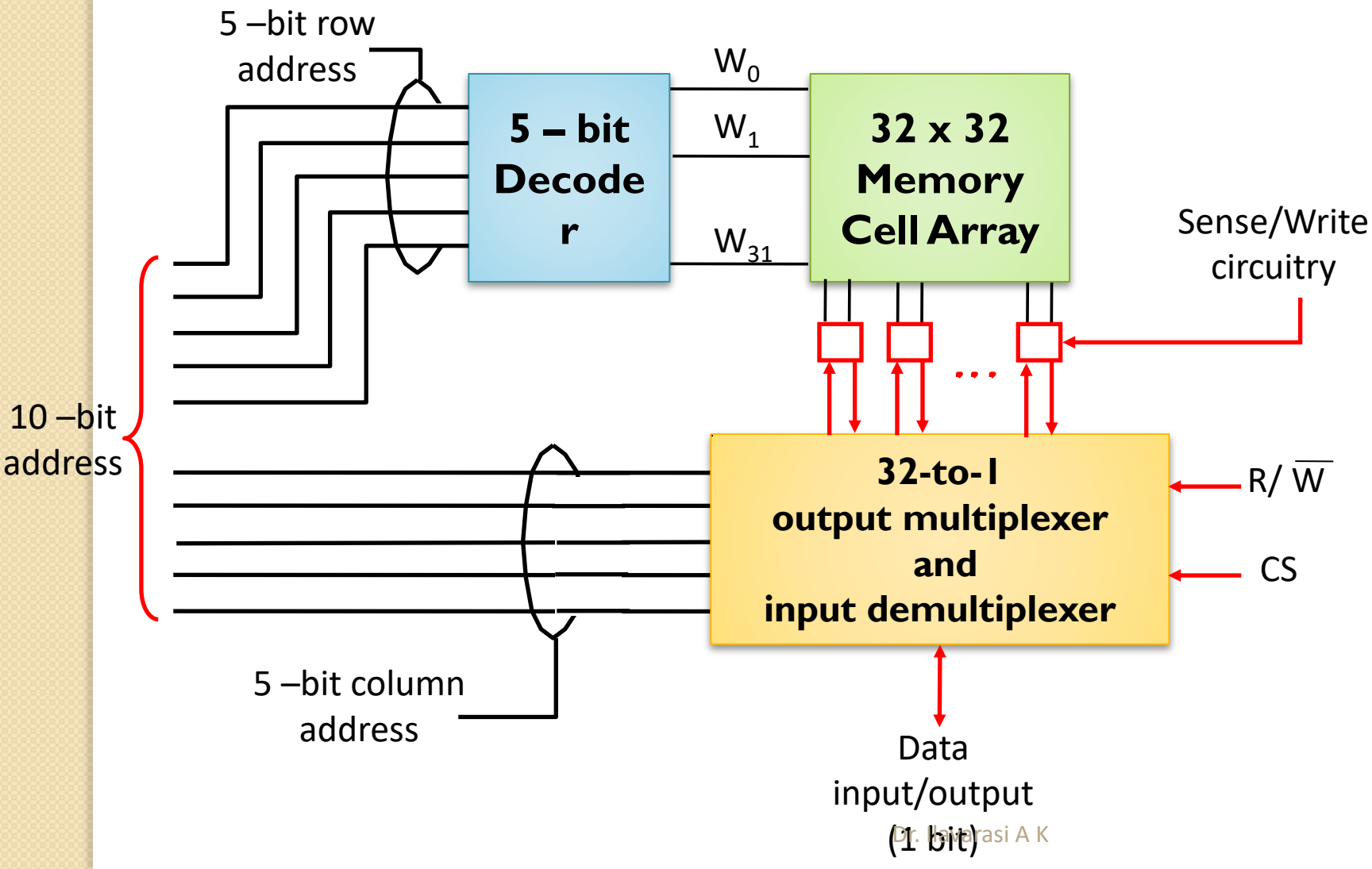


Chip with 1024 Memory Cells

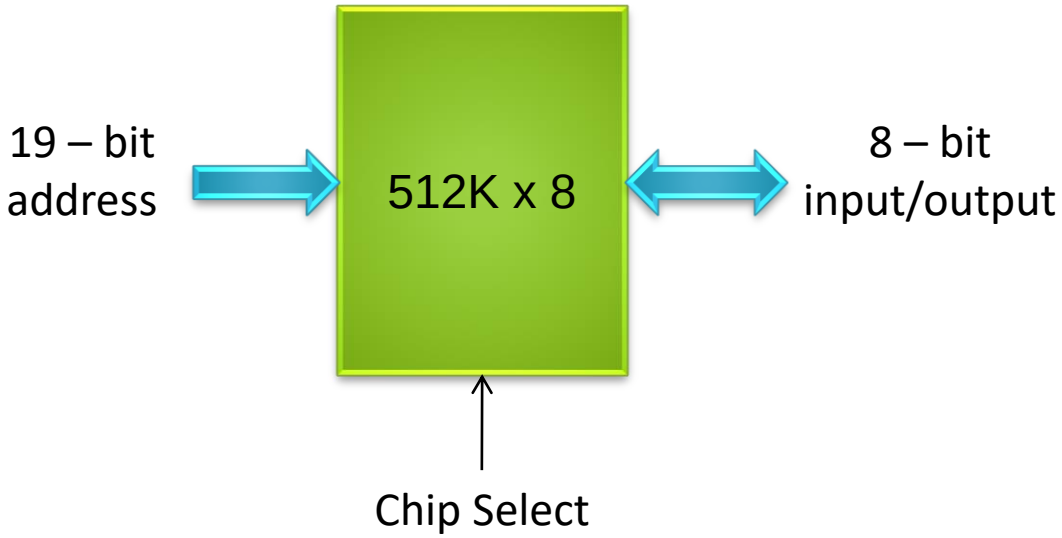
- Or it could be 1024 x 1



Organization of a 1K × 1 memory chip



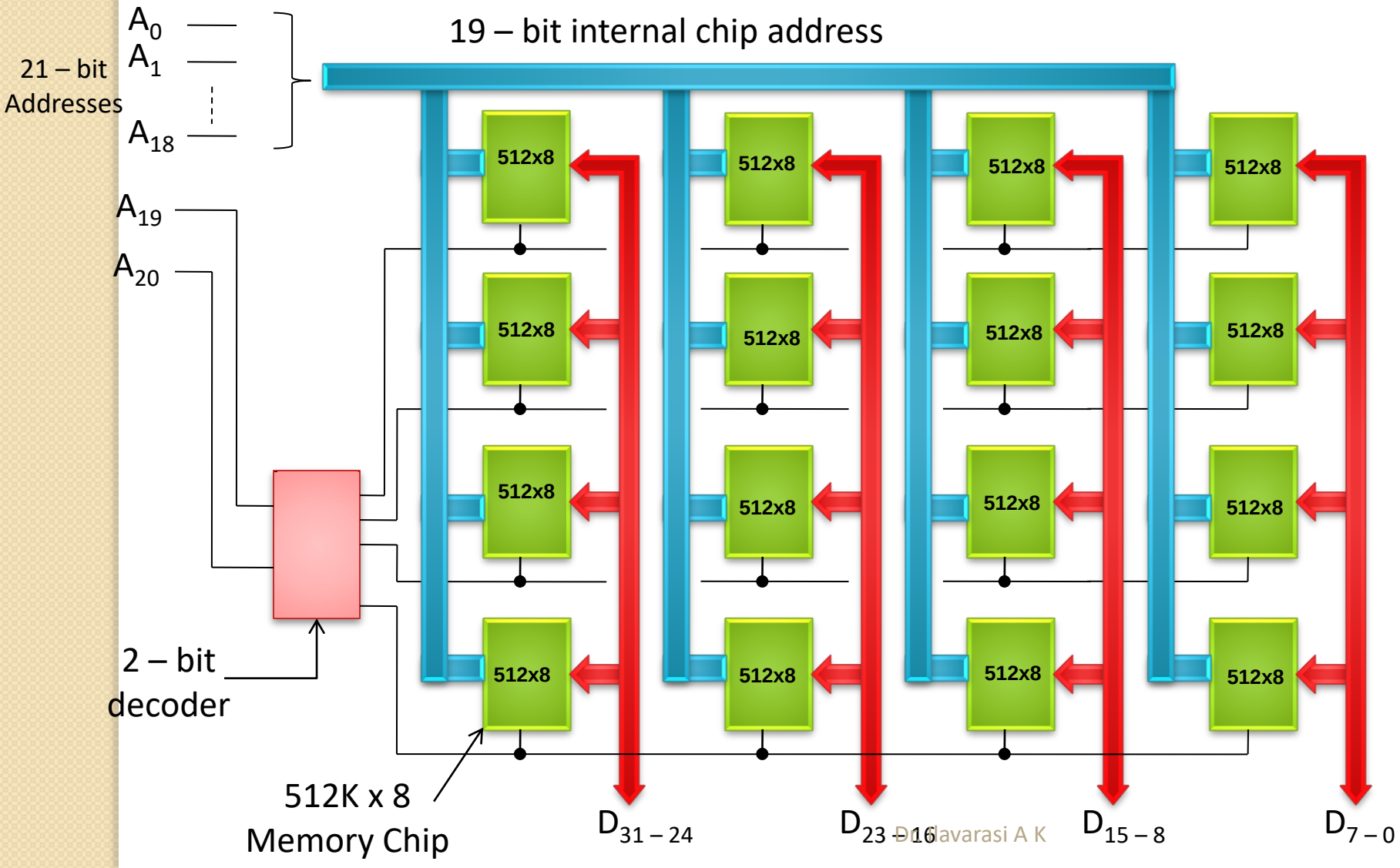
Larger Memories Using Multiple Chips



512K x 8 Memory Chip

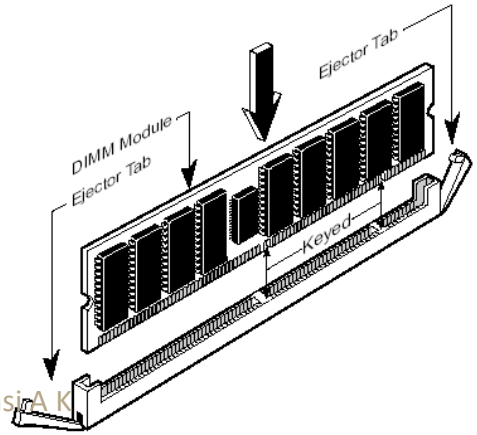
- Organization of a 2M x 32 memory module using 512K x 8 static memory chips
- 2M x 32 ➔ 2 x 2^{10} x 2^{10} x 32 ➔ 2^{21} x 32
- No. of 512K x 8 required = (2^{21} x 32) /(2^{9} x 2^{10} x 8)= 16 nos.

Larger Memories Using Multiple Chips



Larger Memories Using Multiple Chips

- Assembly of several memory chips on a separate small board (PCB) that plugs vertically into a single socket on the motherboard called as Memory Modules
  - SIMMs – Single In-line Memory Modules
  - DIMMs – Dual In-line Memory Modules



Memory System Considerations

- The choice of a RAM chip for a given application depends on several factors
  - Cost,
  - Speed
  - Power dissipation and
  - Size of the chip
- Static RAMs are generally used only when very fast operation is the primary requirement
  - They are used mostly in cache memories
- Dynamic RAMs are the predominant choice for implementing computer main memories